IN THE CLAIMS

Please amend the claims as follows.

1-80. (Canceled)

81. (Previously Presented) A method, comprising:

receiving an F-bit word using J command and address pins of a programmable memory device, wherein F and J are positive integers, wherein J is less than F, wherein the F-bit word comprises a set of command and address signals, and wherein the set of command and address signals consists of an Active command signal, Bank Address signals BA0-BA2, and Row Address signals A0-A11, comprising:

receiving a first portion of the F-bit word at a first time using G command and address pins, wherein the first portion of the F-bit word comprises G-bits, wherein G is less than F, wherein G is less than or equal to J, wherein the first portion of the F-bit word consists of a set of command signals and a first subset of address signals, wherein the set of command signals includes a Chip Select (CS#) signal, a Row Address Strobe (RAS#) signal, a Column Address Strobe (CAS#) signal, and a Write Enable (WE#) signal, wherein receiving the set of command signals includes using a set of Command Pins, wherein the set of Command Pins include a CS# pin, a RAS# pin, a CAS# pin, and a WE# pin, wherein receiving the first subset of address signals includes using a set of Address Pins, and wherein the set of Address Pins include G-4 pins; and

receiving a second portion of the F-bit word at a second time, wherein the second portion of the F-bit word comprises H-bits, wherein H is F-G, wherein H is less than or equal to J, and wherein the second portion of the F-bit word consists of a second subset of address signals; and

performing a memory command in response to the fully-received F-bit word.

82. (Previously Presented) A method, comprising:

receiving an F-bit word using J command and address pins of a programmable memory device, wherein F and J are positive integers, wherein J is less than F, wherein the F-bit word comprises a set of command and address signals, wherein the set of command and address signals consists of an Active command, Bank Address signals, and Row Address signals, and wherein receiving the Active command signal comprises receiving CS# low, RAS# low, CAS# high, and WE# high, comprising:

receiving a first portion of the F-bit word at a first time using G command and address pins, wherein the first portion of the F-bit word comprises G-bits, wherein G is less than F, wherein G is less than or equal to J, wherein the first portion of the F-bit word consists of a set of command signals and a first subset of address signals, wherein the set of command signals includes a Chip Select (CS#) signal, a Row Address Strobe (RAS#) signal, a Column Address Strobe (CAS#) signal, and a Write Enable (WE#) signal, wherein receiving the set of command signals includes using a set of Command Pins, wherein the set of Command Pins include a CS# pin, a RAS# pin, a CAS# pin, and a WE# pin, wherein receiving the first subset of address signals includes using a set of Address Pins, and wherein the set of Address Pins include G-4 pins; and

receiving a second portion of the F-bit word at a second time, wherein the second portion of the F-bit word comprises H-bits, wherein H is F-G, wherein H is less than or equal to J, and wherein the second portion of the F-bit word consists of a second subset of address signals; and

performing a memory command in response to the fully-received F-bit word.

83-91. (Canceled)

92. (Previously Presented) A method, comprising:

receiving an Active command signal, Bank Address signals, and Row Address signals using command and address pins of a programmable memory device, comprising:

receiving the Active command signal, the Bank Address signals, and a first subset of the Row Address signals at a first time using the command and address pins, wherein

the Active command signal includes a Chip Select (CS#) low signal, a Row Address Strobe (RAS#) low signal, a Column Address Strobe (CAS#) high signal, and a Write Enable (WE#) high signal, wherein the CS# signal is received using a CS# command pin, wherein the RAS# signal is received using a RAS# command pin, wherein the CAS# signal is received using a CAS# command pin, and wherein the WE# signal is received using a WE# command pin, wherein the Bank Address signals include BA0-BA2 signals, wherein the BA0 signal is received using a BA0 address pin, wherein the BA1 signal is received using a BA1 address pin, and wherein the BA2 signal is received using a BA2 address pin, and wherein the first subset of Row Address signals includes A11-A9 signals, wherein the A11 signal is received using a A11 address pin, wherein the A10 signal is received using a A10 address pin, and wherein the A9 signal is received using a A9 address pin; and

receiving a second subset of the Row Address signals at a second time using the command and address pins, wherein the second subset of Row Address signals includes A8-A0 signals, wherein the A8 signal is received using the RAS# pin, wherein the A7 signal is received using the CAS# pin, wherein the A6 signal is received using the WE# pin, wherein the A5 signal is received using the BA0 pin, wherein the A4 signal is received using the BA1 pin, wherein the A3 signal is received using the BA2 pin, wherein the A2 signal is received using the A11 pin, wherein the A1 signal is received using the A10 pin, and wherein the A0 signal is received using the A9 pin; and

performing a memory command in response to the fully-received Active command signal, Bank Address signals, and Row Address signals.

93. (Canceled)

94. (Previously Presented) A method, comprising:

receiving an Active command signal, Bank Address signals, and Row Address signals using command and address pins of a programmable memory device, comprising:

receiving the Active command signal, the Bank Address signals, and a first subset of the Row Address signals at a first time using the command and address pins, wherein

the Active command signal includes a Chip Select (CS#) low signal, a Row Address Strobe (RAS#) low signal, a Column Address Strobe (CAS#) high signal, and a Write Enable (WE#) high signal, wherein the CS# signal is received using a CS# command pin, wherein the RAS# signal is received using a RAS# command pin, wherein the CAS# signal is received using a CAS# command pin, and wherein the WE# signal is received using a WE# command pin, wherein the Bank Address signals include BA0-BA2 signals, wherein the BA0 signal is received using a BA0 address pin, wherein the BA1 signal is received using a BA1 address pin, and wherein the BA2 signal is received using a BA2 address pin, and wherein the first subset of Row Address signals includes A12-A8 signals, wherein the A12 signal is received using a A12 address pin, wherein the A11 signal is received using a A11 address pin, wherein the A10 signal is received using a A10 address pin, wherein the A9 signal is received using a A9 address pin, and wherein the A8 signal is received using a A8 address pin; and

receiving a second subset of the Row Address signals at a second time using the command and address pins, wherein the second subset of Row Address signals includes A7-A0 signals, wherein the A7 signal is received using the BA0 pin, wherein the A6 signal is received using the BA1 pin, wherein the A5 signal is received using the BA2 pin, wherein the A4 signal is received using the A12 pin, wherein the A3 signal is received using the A11 pin, wherein the A2 signal is received using the A10 pin, wherein the A1 signal is received using the A9 pin, and wherein the A0 signal is received using the A8 pin; and

performing a memory command in response to the fully-received Active command signal, Bank Address signals, and Row Address signals.

95. (Canceled)

96. (Previously Presented) The method of claim 81, wherein a first time includes at or substantially simultaneously with receiving a first rising edge of a first cycle of a clock signal.

97. (Previously Presented) The method of claim 81, wherein the first time includes at or substantially simultaneously with receiving a first falling edge of a first cycle of a clock signal.

98. (Previously Presented) The method of claim 81, wherein a second time includes at or substantially simultaneously with receiving a first rising edge of a second cycle of a clock signal.

99. (Previously Presented) The method of claim 81, wherein the second time includes at or substantially simultaneously with receiving a first falling edge of a second cycle of a clock signal.

100. (Previously Presented) The method of claim 81, wherein the performing the memory command includes performing a block read in a static memory device.

101. (Previously Presented) The method of claim 81, wherein the programmable memory device includes a volatile memory device.

102. (Previously Presented) The method of claim 81, further comprising:
sending the first portion of the F-bit word with a controller at a first time; and
sending the second portion of the F-bit word with a controller at a second time.

103. (Previously Presented) The method of claim 102, wherein the controller includes a processor.

104. (Previously Presented) The method of claim 102, wherein the first time includes at or substantially simultaneously with receiving a first rising edge of a first cycle of a clock signal.

105. (Previously Presented) The method of claim 102, wherein the first time includes at or substantially simultaneously with receiving a first falling edge of a first cycle of a clock signal.

106. (Previously Presented) The method of claim 102, wherein the second time includes at or substantially simultaneously with receiving a first rising edge of a second cycle of a clock signal.

107. (Previously Presented) The method of claim 102, wherein the second time includes at or substantially simultaneously with receiving a first falling edge of a second cycle of a clock signal.

108. (Previously Presented) The method of claim 81, wherein H and G are not equal to each other.

109. (Previously Presented) The method of claim 81, wherein the programmable memory device consists of J command and address pins.

110. (Previously Presented) The method of claim 81, wherein receiving the second subset of address signals includes using at least one of the set of Address Pins.

111. (Previously Presented) The method of claim 81, wherein receiving the second subset of address signals includes using at least one Command Pin and at least one Address Pin.

112. (Previously Presented) The method of claim 111, wherein using the at least one Command Pin and the at least one Address Pin include using H command and address pins, wherein H is greater than G-4.

113. (Previously Presented) The method of claim 111, wherein the at least one Command Pin includes at least one of the RAS# pin, the CAS # pin, and the WE# pin.

114. (Canceled)

115. (Previously Presented) The method of claim 82, wherein a first time includes at or substantially simultaneously with receiving a first rising edge of a first cycle of a clock signal.

116. (Previously Presented) The method of claim 82, wherein the first time includes at or substantially simultaneously with receiving a first falling edge of a first cycle of a clock signal.

117. (Previously Presented) The method of claim 82, wherein a second time includes at or substantially simultaneously with receiving a first rising edge of a second cycle of a clock signal.

118. (Previously Presented) The method of claim 82, wherein the second time includes at or substantially simultaneously with receiving a first falling edge of a second cycle of a clock signal.

119. (Previously Presented) The method of claim 82, wherein performing the memory command includes performing a write in a static memory device.

120. (Previously Presented) The method of claim 82, wherein the programmable memory device includes a volatile memory device.

121. (Previously Presented) The method of claim 82, further comprising:
sending the first portion of the F-bit word with a controller at a first time; and
sending the second portion of the F-bit word with a controller at a second time.

122. (Previously Presented) The method of claim 121, wherein the controller includes a processor.

123. (Previously Presented) The method of claim 121, wherein the first time includes at or substantially simultaneously with receiving a first rising edge of a first cycle of a clock signal.

124. (Previously Presented) The method of claim 121, wherein the first time includes at or substantially simultaneously with receiving a first falling edge of a first cycle of a clock signal.

125. (Previously Presented) The method of claim 121, wherein the second time includes at or substantially simultaneously with receiving a first rising edge of a second cycle of a clock signal.

126. (Previously Presented) The method of claim 121, wherein the second time includes at or substantially simultaneously with receiving a first falling edge of a second cycle of a clock signal.

127. (Previously Presented) The method of claim 82, wherein H and G are not equal to each other.

128. (Previously Presented) The method of claim 82, wherein the programmable memory device consists of J command and address pins.

129. (Previously Presented) The method of claim 82, wherein receiving the second subset of address signals includes using at least one of the set of Address Pins.

130. (Previously Presented) The method of claim 129, wherein receiving the second subset of address signals includes using at least one Command Pin.

131. (Previously Presented) The method of claim 130, wherein using the at least one Command Pin and the at least one Address Pin include using H command and address pins, wherein H is greater than G-4.

132. (Previously Presented) The method of claim 130, wherein the at least one Command Pin includes at least one of the RAS# pin, the CAS# pin, and the WE# pin.

133. (Canceled)

134. (Previously Presented) The method of claim 92, wherein a first time includes at or substantially simultaneously with receiving a first rising edge of a first cycle of a clock signal.

135. (Previously Presented) The method of claim 92, wherein the first time includes at or substantially simultaneously with receiving a first falling edge of a first cycle of a clock signal.

136. (Previously Presented) The method of claim 92, wherein a second time includes at or substantially simultaneously with receiving a first rising edge of a second cycle of a clock signal.

137. (Previously Presented) The method of claim 92, wherein the second time includes at or substantially simultaneously with receiving a first falling edge of a second cycle of a clock signal.

138. (Previously Presented) The method of claim 92, wherein the performing the memory command includes performing a block erase in a static memory device.

139. (Previously Presented) The method of claim 92, wherein the programmable memory device includes a volatile memory device.

140. (Currently Amended) The method of claim 92, further comprising:

sending the ~~first portion of the F-bit word~~ Active command signal, the Bank Address signals, and the first subset of the Row Address signals with a controller at a first time; and

sending the ~~second portion of the F-bit word~~ second subset of the Row Address signals with a controller at a second time.

141. (Previously Presented) The method of claim 140, wherein the controller includes a processor.

142. (Previously Presented) The method of claim 140, wherein the first time includes at or substantially simultaneously with receiving a first rising edge of a first cycle of a clock signal.

143. (Previously Presented) The method of claim 140, wherein the first time includes at or substantially simultaneously with receiving a first falling edge of a first cycle of a clock signal.

144. (Previously Presented) The method of claim 140, wherein the second time includes at or substantially simultaneously with receiving a first rising edge of a second cycle of a clock signal.

145. (Previously Presented) The method of claim 140, wherein the second time includes at or substantially simultaneously with receiving a first falling edge of a second cycle of a clock signal.

146. (Currently Amended) The method of claim 92, wherein ~~H~~ the number of bits in the Active command signal, the Bank Address signals, and the first subset of the Row Address signals ~~and G~~ are not equal to ~~each other~~ the number of bits in the second subset of the Row Address signals.

147. (Canceled)

148. (Previously Presented) The method of claim 94, wherein a first time includes at or substantially simultaneously with receiving a first rising edge of a first cycle of a clock signal.

149. (Previously Presented) The method of claim 94, wherein the first time includes at or substantially simultaneously with receiving a first falling edge of a first cycle of a clock signal.

150. (Previously Presented) The method of claim 94, wherein a second time includes at or substantially simultaneously with receiving a first rising edge of a second cycle of a clock signal.

151. (Previously Presented) The method of claim 94, wherein the second time includes at or substantially simultaneously with receiving a first falling edge of a second cycle of a clock signal.

152. (Previously Presented) The method of claim 94, wherein the performing the memory command includes performing a block erase in a static memory device.

153. (Previously Presented) The method of claim 94, wherein the programmable memory device includes a volatile memory device.

154. (Currently Amended) The method of claim 94, further comprising:

sending the ~~first portion of the F-bit word~~ Active command signal, the Bank Address signals, and the first subset of the Row Address signals with a controller at a first time; and

sending the ~~second portion of the F-bit word~~ second subset of the Row Address signals with a controller at a second time.

155. (Previously Presented) The method of claim 154, wherein the controller includes a processor.

156. (Previously Presented) The method of claim 154, wherein the first time includes at or substantially simultaneously with receiving a first rising edge of a first cycle of a clock signal.

157. (Previously Presented) The method of claim 154, wherein the first time includes at or substantially simultaneously with receiving a first falling edge of a first cycle of a clock signal.

158. (Previously Presented) The method of claim 154, wherein the second time includes at or substantially simultaneously with receiving a first rising edge of a second cycle of a clock signal.

159. (Currently Amended) The method of claim ~~158~~154, wherein the second time includes at or substantially simultaneously with receiving a first falling edge of a second cycle of a clock signal.

160. (Currently Amended) The method of claim 94, wherein ~~H~~ the number of bits in the Active command signal, the Bank Address signals, and the first subset of the Row Address signals ~~and G~~ are not equal to ~~each other~~ the number of bits in the second subset of the Row Address signals.

161. (Canceled)